COL215 Mini-Project Report

CRC-CCITT Computation

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**Detailed description of the overall design**

We have planned to tackle the problem by making a Moore Finite State Machine.

The FSM contains 3 states.

1. Loading value from switches to the registers i.e. poly = crc polynomial, data=1111111111111111&input&0000000000000000, counter = 0000, crc = data(47 downto 31), done=0
2. Repeated XOR process till we finally obtain our CRC Value.

Pseudo code:

if (counter=1111)

state=3

done=1

If (counter!=0000)

shift data left;

(data(47 downto 31))xor(poly);

conter += 1;

1. Reset function that outputs seed value to the CRC.

**Description of the major subsystems/components and interconnecting signals**

counter = 0 to 15 to count xor operations

done = 0 or 1 indicating computation done or not

data = register

polynomial = crc polynomial

state = 1 or 2 or 3

load = if 1 load values

reset = if 1 set data to seed value

**Status of coding**

We have coded the Moore FSM (output values are determined only by its current state) first time, might have flaws. The whole machine is a one process machine that is purely sequential. We still have to modify SSD code suiting the requirements.

**Status of testing**

We have remove all synthesis related error like buss size mismatch in the computation part